

# Characterization of an Mg-implanted GaN p-i-n Diode

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**Abstract:** A p-i-n diode formed by the implantation of Mg in GaN was fabricated and characterized. After implantation, Mg was activated using the symmetrical multicycle rapid thermal annealing technique with heating pulses up to 1340°C. The Mg-implanted p-i-n diode exhibits rectification and low leakage currents. The realization of an Mg-implanted GaN device is a key step for future power electronic devices.

**Keywords:** GaN, p-i-n diode, ion implantation

## Introduction

III-nitride materials have attracted a continuous interest due to their wide range of applications, including optoelectronic, power electronic, and extreme environments. Several high impact devices, including the blue LED, have been implemented using the III-nitride material system. Unfortunately, the ability to implant and activate dopants in III-nitride materials is not well understood, and it is a key technical impediment to true planar processing in the III-nitride material system. Devices such as the current aperture vertical electron transistor (CAVET), Schottky diodes with guard ring termination or grayscale junction termination extension, and vertical p-i-n diodes will be enhanced and enabled by the ability to selectively dope GaN without the need for etching or regrowth [1-4]. Here, we report on the characterization of implanted p-i-n diodes fabricated on a bulk GaN material.

## Device Fabrication

A 10  $\mu\text{m}$  thick unintentionally doped GaN layer was grown by metal organic chemical vapor deposition (MOCVD) on a  $\text{n}^+$  Ga-face c-oriented GaN substrate. The as-grown MOCVD film is smooth and exhibits step flow growth indicative of high quality epitaxial GaN. The p-GaN anode and termination regions were formed by Mg implantation to a concentration of  $2 \times 10^{19} \text{ cm}^{-3}$  following a box profile to a depth of 500nm. A photoresist mask was used for the implantation, aligned to zero level marks etched 100nm into the GaN by  $\text{Cl}_2$ -based inductively coupled plasma (ICP) etching. The implanted dopants were activated using the symmetric multicycle rapid thermal annealing (SMRTA) technique described later [5]. After activation by SMRTA to a maximum temperature of 1410 °C and removal of the sputtered AlN protective cap structure using AZ400K

[6], The anode metal was formed by lift-off of Pd/Au (20/100nm), followed by rapid thermal annealing in a  $\text{N}_2$  atmosphere, and the cathode metal was a blanket film of e-beam deposited Al on the back side of the sample. A schematic of the device structure is shown in Figure 1.

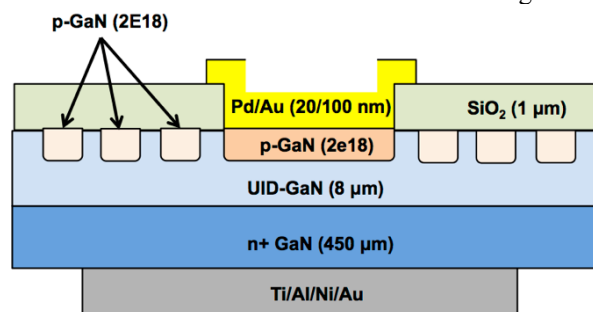
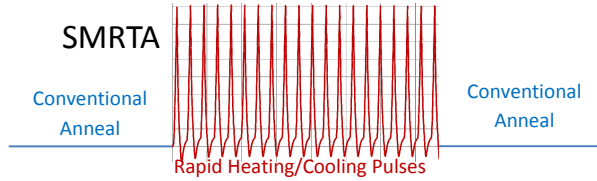


Figure 1. Device Cross Section

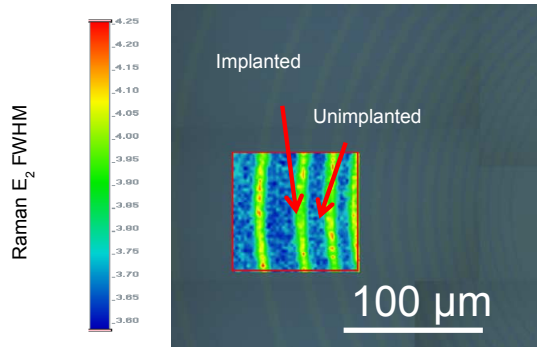
The activation of implanted dopants in GaN has two separate requirements. First, the damage created by the implantation must be reversed. Secondly, the implanted ions must be given enough energy to migrate to their proper lattice sites. In the case of Mg implanted GaN, the Mg must replace Ga to result in p-type material. In many other semiconductor materials such as Si and SiC, ion implantation is a routine step in most processing sequences. In GaN, the activation of implanted dopants is more difficult and has been the subject of intense research. This difficulty arises from the high temperatures to achieve p-type doping after implantation ( $>1300^\circ\text{C}$ ). GaN begins to decompose at around  $840^\circ\text{C}$  at atmospheric pressures, creating a gap of over  $450^\circ\text{C}$  between the temperatures needed to activate p-type dopants and the decomposition temperature of GaN.

Several methods have been attempted to achieve the high temperature annealing of GaN. One method is to utilize a high nitrogen overpressures of over 10,000 bar during the annealing process to avoid decomposition. Using this high nitrogen overpressure has been successfully demonstrated as a method to anneal GaN at temperatures up to  $1500^\circ\text{C}$ . [6] The pressures required are prohibitively high and require specialized equipment that is not easily industrial scalable. Capping materials have also been shown to extend the range of decomposition in GaN. AlN has shown the most promise as a capping material, and has facilitated the annealing of GaN up to  $1100^\circ\text{C}$ .

In this research, we utilize a combination of the two approaches, including the use of an optimized annealing scheme - symmetric multicycle rapid thermal annealing (SMRTA) as shown in Figure 2, which includes two conventional anneals performed at thermodynamically stable temperatures with rapid heating and cooling pulses sandwiched between in addition to an optimized capping structure. [2] We also use a moderate nitrogen overpressure of 24 bar. Using this annealing technique, a vertical GaN pin diode structure was implemented. The crystal quality of the GaN before and after the annealing process was observed using Raman spectroscopy mapping as shown in Figure 3. It was determined that the FWHM of the GaN  $E_2$  mode increases after the implantation process, consistent with crystalline damage. The FWHM of the GaN  $E_2$  mode before and after implantation are 3.79 and 4.11  $\text{cm}^{-1}$ , respectively. After annealing with 20 pulses to 1350  $^{\circ}\text{C}$ , the crystalline quality was probed using Raman spectroscopy, and the FWHM of the implanted region decreased from 4.11  $\text{cm}^{-1}$  to 3.81  $\text{cm}^{-1}$ .



**Figure 2.** A schematic of the SMRTA process, which is composed of two conventional annealing steps with rapid heating and cooling pulses between the conventional annealing steps.



**Figure 3.** Raman map for the as-implanted pin structure.

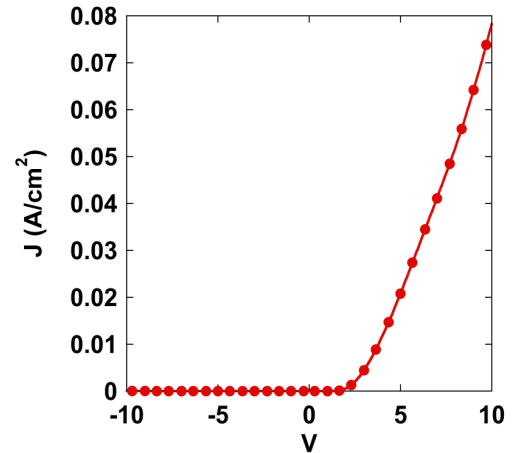
Before the SMRTA annealing process, the FWHM of the GaN  $E_2$  mode in the implanted portion of the sample is 4.11  $\text{cm}^{-1}$ . After annealing, the crystal quality recovers as evident by a GaN  $E_2$  mode FWHM of 3.81  $\text{cm}^{-1}$ .

Upon optical inspection of the devices after capping for SMRTA, cracking was initially observed. Several problems arise in capping bulk GaN that are not present in capping heteroepitaxial GaN on sapphire films where the cap and SMRTA process was initially developed. First, both the front and back of the substrates need to be encapsulated to prevent GaN decomposition during

SMRTA. Second, it was determined that cracking of AlN occurs on epi-ready face under elevated temperature sputtering conditions ( $T_{\text{sub}} = 400\text{ }^{\circ}\text{C}$ ). This cracking did not occur on heteroepitaxial surfaces that were rougher than the polished bulk GaN surfaces (i.e. optical polish). Cracking happens with both thick and thin sputtered AlN and is due to the lattice mismatch between GaN and AlN. The cracking was effectively mitigated by employing an optimized capping structure for bulk GaN samples using low temperature sputtered AlN. [8]

### Electrical Testing & Analysis

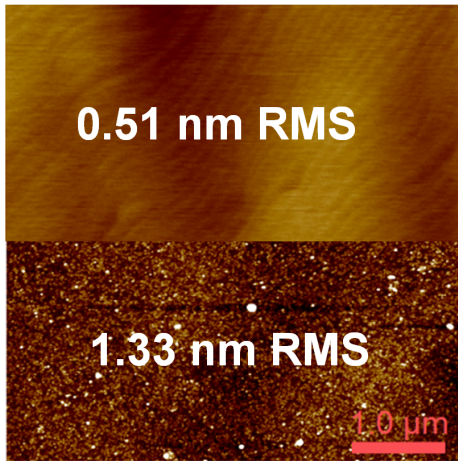
Rectifying behavior was observed, as shown in Figure 3 for the device with the optimized cap. This represents a first for a p-i-n structure formed by Mg ion implantation in GaN. The turn-on voltage is consistent with a p-n junction, and the ideality factor of 2.6 is consistent with a recombination/generation-based transport mechanism. Non-ideal behavior is associated with recombination in the drift layer due to crystalline defects. The devices suffer from high ON-resistance due to high contact resistance and recombination in the drift layer, which limited the forward current to 1  $\text{A}/\text{cm}^2$ . Capacitance-voltage measurements indicated the presence of a p-GaN layer, with a depletion layer thickness  $\sim 500\text{ nm}$  and a doping density of  $2 \times 10^{18}\text{ cm}^{-3}$ , corresponding to an activation ratio of 10%. The On/Off ratio at  $\pm 10\text{ V}$  was  $10^6$ .



**Figure 4.** I-V curve of the vertical Mg-implanted GaN pin. The turn on voltage is around 3 V with an on/off ratio of over  $10^6$ .

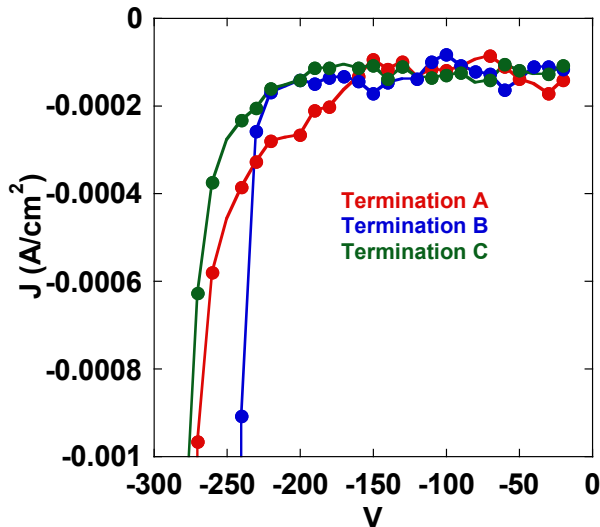
To further probe the nonideal diode behavior, we investigated the properties of the drift layer after processing. An AFM investigation of the surface after device processing indicated an increase in surface roughness from, 0.51 nm to 1.33 nm, as shown in Figure 5. This was traced to the capping process, which involved a 10W plasma clean prior to sputtering. As plasma damage in GaN is typically N-type, this was identified as the source of high contact resistance due to type inversion. Modification to the process resulted in preservation of the

smooth, stepped surface through the entire fabrication sequence.



**Figure 5.** Atomic force microscope image of the GaN surface before (top) and after (bottom) a 10 W plasma clean used prior to the AlN cap deposition.

Blocking tests, indicate a breakdown voltage of  $\sim 300\text{V}$  based on a criteria of  $J=1\text{ mA/cm}^2$ . The breakdown voltage was independent of termination design, as shown in Figure 6. The optimized capping process significantly improved reverse leakage, further improving on/off ratio by several orders of magnitude. However, the breakdown voltage was not improved and appears low for the thickness of the drift layer. This implies that either the background doping in the drift region is too high or the critical field is low due to damage from the ion implantation.



**Figure 6.** Blocking measurements on devices with and without optimized cap process

## Conclusions

An ion implanted GaN p-i-n diode enabled by the symmetric multicycle rapid thermal annealing technique was demonstrated. The capping structure was optimized to avoid cracking of the AlN layer as well as eliminate plasma damage to the GaN surface. Electrical characterization exhibited rectifying behavior with low reverse leakage current and forward characteristics consistent with a GaN p-n junction. The breakdown voltage is still low due to either high background doping in the drift region or a low critical field due to a defective GaN layer near the junction and possibly in the depletion region. The ability to integrate p-type GaN layers in planar device structures by ion implantation represents a significant step for next-generation power devices.

## Acknowledgments

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